**DataFlow**

**Verilog Module:**

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 21:53:38 10/16/2022

// Design Name:

// Module Name: AND

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

//2020-CE-121 Zahir Khan

module Dataflow( //Dataflow

input a,

input b,

input c,

output y

);

assign y = (((a&b)&c)|((a&b)&(~c)));

endmodule

**TEXT FIXTURE:**

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 12:44:51 01/23/2023

// Design Name: AND

// Module Name: D:/Xilinx/Workspace/Dataflow/TF.v

// Project Name: Lab1

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: AND

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module TF;

// Inputs

reg a;

reg b;

reg c;

// Outputs

wire y;

// Instantiate the Unit Under Test (UUT)

Dataflow uut (

.a(a),

.b(b),

.c(c),

.y(y)

);

initial begin

// Wait 100 ns for global reset to finish

// Initialize Inputs

a = 0;

b = 0;

c = 0;

// Wait 100 ns for global reset to finish

#100;

a = 0;

b = 0;

c = 1;

#100;

a = 0;

b = 1;

c = 0;

#100;

a = 0;

b = 1;

c = 1;

#100;

a = 1;

b = 0;

c = 0;

#100;

a = 1;

b = 0;

c = 1;

#100;

a = 1;

b = 1;

c = 0;

#100;

a = 1;

b = 1;

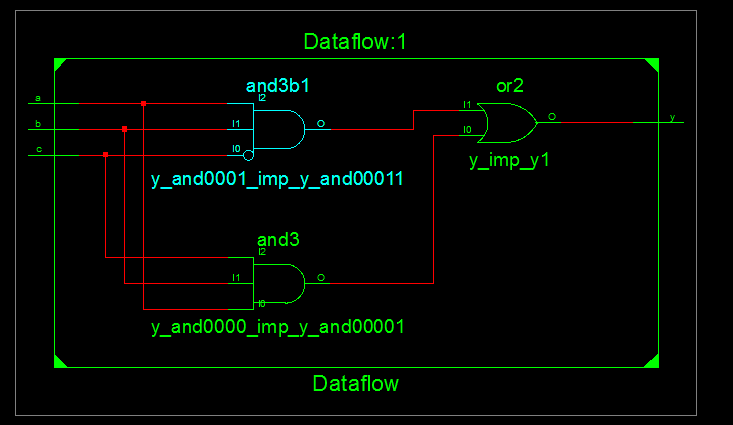
c = 1;

// Add stimulus here

end

endmodule

**SCHEMATIC:**



**WaveForm:**

